# 7

# Insulated Gate Bipolar Transistor (IGBT)

**Constructional features, operating principle and characteristics of Insulated Gate Bipolar Transistors (IGBT)**

# Instructional objects

On completion the student will be able to

- Differentiate between the constructional features of an IGBT and a MOSFET.
- Draw the operational equivalent circuit of an IGBT and explain its operating principle in terms of the schematic construction and the operational equivalent circuit.
- Draw and explain the steady state output and transfer characteristics of an IGBT.
- Draw the switching characteristics of an IGBT and identify its differences with that of a MOSFET.
- Design a basic gate drive circuit for an IGBT.
- Interpret the manufacturer's date sheet of an IGBT.

## 7.1 Introduction

The introduction of Power MOSFET was originally regarded as a major threat to the power bipolar transistor. However, initial claims of infinite current gain for the power MOSFETs were diluted by the need to design the gate drive circuit capable of supplying the charging and discharging current of the device input capacitance. This is especially true in high frequency circuits where the power MOSFET is particularly valuable due to its inherently high switching speed. On the other hand, MOSFETs have a higher on state resistance per unit area and consequently higher on state loss. This is particularly true for higher voltage devices (greater than about 500 volts) which restricted the use of MOSFETs to low voltage high frequency circuits (eg. SMPS).

With the discovery that power MOSFETs were not in a strong position to displace the BJT, many researches began to look at the possibility of combining these technologies to achieve a hybrid device which has a high input impedance and a low on state resistance. The obvious first step was to drive an output **npn** BJT with an input MOSFET connected in the Darlington configuration. However, this approach required the use of a high voltage power MOSFET with considerable current carrying capacity (due to low current gain of the output transistor). Also, since no path for negative base current exists for the output transistor, its turn off time also tends to get somewhat larger. An alternative hybrid approach was investigated at GE Research center where a MOS gate structures was used to trigger the latch up of a four layer thyristor. However, this device was also not a true replacement of a BJT since gate control was lost once the thyristor latched up.

After several such attempts it was concluded that for better results MOSFET and BJT technologies are to be integrated at the cell level. This was achieved by the GE Research Laboratory by the introduction of the device IGT and by the RCA research laboratory with the device COMFET. The IGT device has undergone many improvement cycles to result in the modern Insulated Gate Bipolar Transistor (IGBT). These devices have near ideal characteristics for high voltage (> 100V) medium frequency (< 20 kHZ) applications. This device along with the MOSFET (at low voltage high frequency applications) have the potential to replace the BJT completely.

## 7.2 Constructional Features of an IGBT

Vertical cross section of a n channel IGBT cell is shown in Fig 7.1. Although p channel IGBTs are possible n channel devices are more common and will be the one discussed in this lesson.

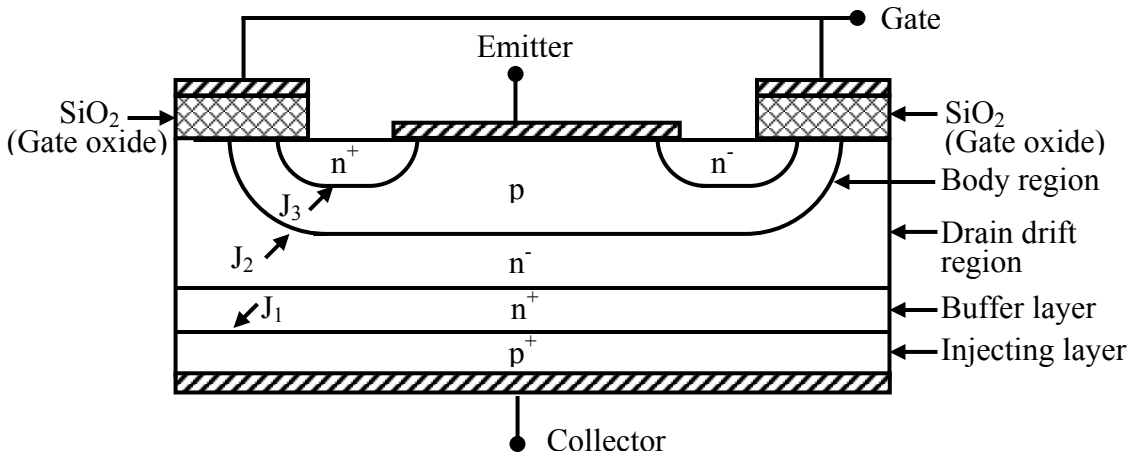



**Fig. 7.1: Vertical cross section of an IGBT cell.**

The major difference with the corresponding MOSFET cell structure lies in the addition of a **p+** injecting layer. This layer forms a **pn** junction with the drain layer and injects minority carriers into it. The **n** type drain layer itself may have two different doping levels. The lightly doped **n-** region is called the drain drift region. Doping level and width of this layer sets the forward blocking voltage (determined by the reverse break down voltage of $J_2$) of the device. However, it does not affect the on state voltage drop of the device due to conductivity modulation as discussed in connection with the power diode. This construction of the device is called "Punch Trough" (PT) design. The Non-Punch Through (NPT) construction does not have this added **n+** buffer layer. The PT construction does offer lower on state voltage drop compared to the NPT construction particularly for lower voltage rated devices. However, it does so at the cost of lower reverse break down voltage for the device, since the reverse break down voltage of the junction $J_1$ is small. The rest of the construction of the device is very similar to that of a **vertical MOSFET** **(Link to 6.2)** including the insulated gate structure and the shorted body (**p** type) – emitter (**n+** type) structure. The doping level and physical geometry of the **p** type body region however, is considerably different from that of a MOSFET in order to defeat the latch up action of a parasitic thyristor embedded in the IGBT structure. A large number of basic cells as shown in Fig 7.1 are grown on a single silicon wafer and connected in parallel to form a complete IGBT device.

The IGBT cell has a parasitic **p-n-p-n** thyristor structure embedded into it as shown in Fig 7.2(a). The constituent **p-n-p** transistor, **n-p-n** transistor and the driver MOSFET are shown by dotted lines in this figure. Important resistances in the current flow path are also indicated.

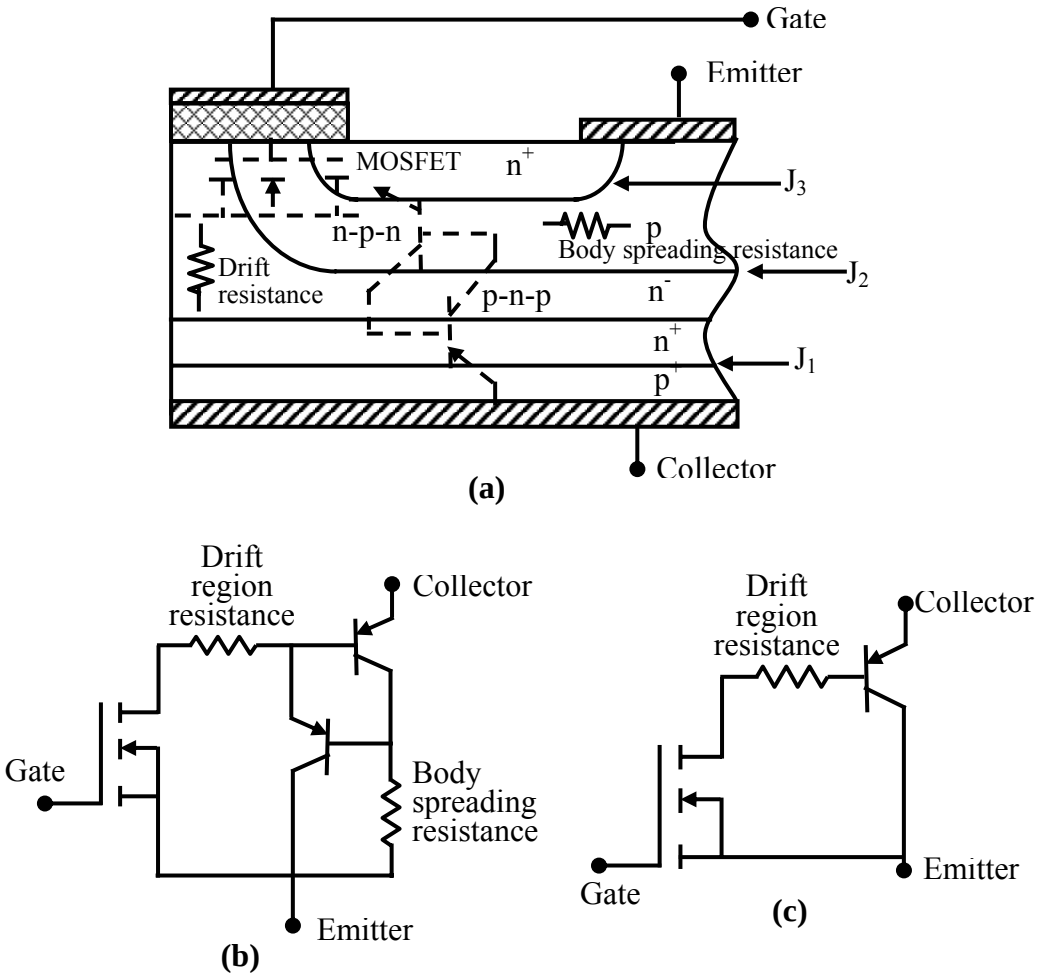



**Fig. 7.2: Parasitic thyristor in an IGBT cell.**
**(a) Schematic structure**
**(b) Exact equivalent circuit.**
**(c) Approximate equivalent circuit**

Fig 7.2(b) shows the exact static equivalent circuit of the IGBT cell structure. The top **p-n-p** transistor is formed by the **p+** injecting layer as the emitter, the **n** type drain layer as the base and the **p** type body layer as the collector. The lower **n-p-n** transistor has the **n+** type source, the **p** type body and the **n** type drain as the emitter, base and collector respectively. The base of the lower **n-p-n** transistor is shorted to the emitter by the emitter metallization. However, due to imperfect shorting, the exact equivalent circuit of the IGBT includes the body spreading resistance between the base and the emitter of the lower **n-p-n** transistor. If the output current is large enough, the voltage drop across this resistance may forward bias the lower **n-p-n** transistor and initiate the latch up process of the **p-n-p-n** thyristor structure. Once this structure latches up the gate control of IGBT is lost and the device is destroyed due to excessive power loss.

A major effort in the development of IGBT has been towards prevention of latch up of the parasitic thyristor. This has been achieved by modifying the doping level and physical geometry of the body region. The modern IGBT is latch-up proof for all practical purpose. Fig 7.3(a) and (b) shows the circuit symbol and photograph of an IGBT.

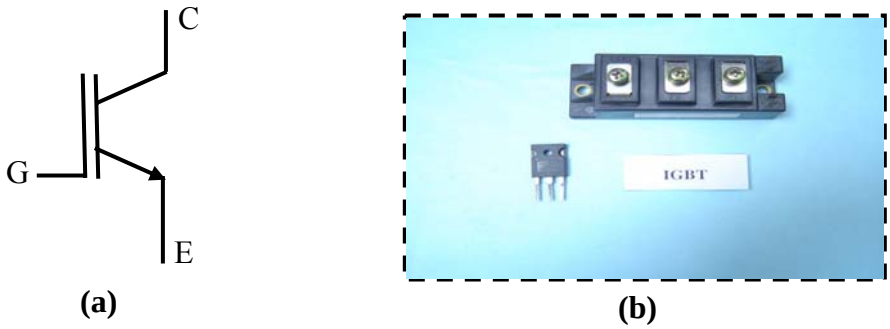



**Fig. 7.3: Circuit symbol of an IGBT.**
**(a) Circuit symbol.**
**(b) Photograph.**

**Exercise 7.1**

Fill in the blank(s) with the appropriate word(s).

i. An IGBT is a _____ device combining the advantages of a _____ and a _____.

ii. IGBT is suitable for _____ voltage _____ frequency applications.

iii. In an IGBT cell structure a _____ type injecting layer is added on top of the drain of an **n** channel MOSFET.

iv. The forward blocking voltage of an IGBT is determined by the _____ and _____ of the drain drift layer.

v. A "punch through" IGBT has _____ reverse break down voltage while the "Non punch through" IGBT has _____ voltage blocking capacity.

vi. The IGBT cell has a parasitic _____ structure embedded into it.

vii. The parasitic _____ structure of an IGBT cell can _____ at large collector current due to imperfect body emitter shorting.

viii. The doping level and physical geometry of the IGBT _____ region is designed to be considerably different from that of a MOSFET to prevent its _____.

**Answers:**
i) hybrid, MOSFET, BJT ; ii) high, medium ; iii) **p+** ; iv) thickness, doping level ; v) low, symmetrical ; vi) thyristor; vii) thryistor, latch up ; viii) body, latch up.

## 7.3 Operating principle of an IGBT

Operating principle of an IGBT can be explained in terms of the schematic cell structure and equivalent circuit of Fig 7.2(a) and (c). From the input side the IGBT behaves essentially as a

MOSFET. Therefore, when the gate emitter voltage is less then the threshold voltage no inversion layer is formed in the **p** type body region and the device is in the off state. The forward voltage applied between the collector and the emitter drops almost entirely across the junction $J_2$. Very small leakage current flows through the device under this condition. In terms of the equivalent current of Fig 7.2(c), when the gate emitter voltage is lower than the threshold voltage the driving MOSFET of the Darlington configuration remains off and hence the output **p-n-p** transistor also remains off.

When the gate emitter voltage exceeds the threshold, an inversion layer forms in the **p** type body region under the gate. This inversion layer (channel) shorts the emitter and the drain drift layer and an electron current flows from the emitter through this channel to the drain drift region. This in turn causes substantial hole injection from the **p+** type collector to the drain drift region. A portion of these holes recombine with the electrons arriving at the drain drift region through the channel. The rest of the holes cross the drift region to reach the p type body where they are collected by the source metallization.

From the above discussion it is clear that the n type drain drift region acts as the base of the output **p-n-p** transistor. The doping level and the thickness of this layer determines the current gain "$\propto$" of the **p-n-p** transistor. This is intentionally kept low so that most of the device current flows through the MOSFET and not the output **p-n-p** transistor collector. This helps to reduced the voltage drop across the "body" spreading resistance shown in Fig 7.2 (b) and eliminate the possibility of static latch up of the IGBT.

The total on state voltage drop across a conducting IGBT has three components. The voltage drop across $J_1$ follows the usual exponential law of a **pn** junction. The next component of the voltage drop is due to the drain drift region resistance. This component in an IGBT is considerably lower compared to a MOSFET due to strong conductivity modulation by the injected minority carriers from the collector. This is the main reason for reduced voltage drop across an IGBT compared to an equivalent MOSFET. The last component of the voltage drop across an IGBT is due to the channel resistance and its magnitude is equal to that of a comparable MOSFET.

## 7.4 Steady state characteristics of an IGBT

The i-v characteristics of an n channel IGBT is shown in Fig 7.4 (a). They appear qualitatively similar to those of a logic level BJT except that the controlling parameter is not a base current but the gate-emitter voltage.

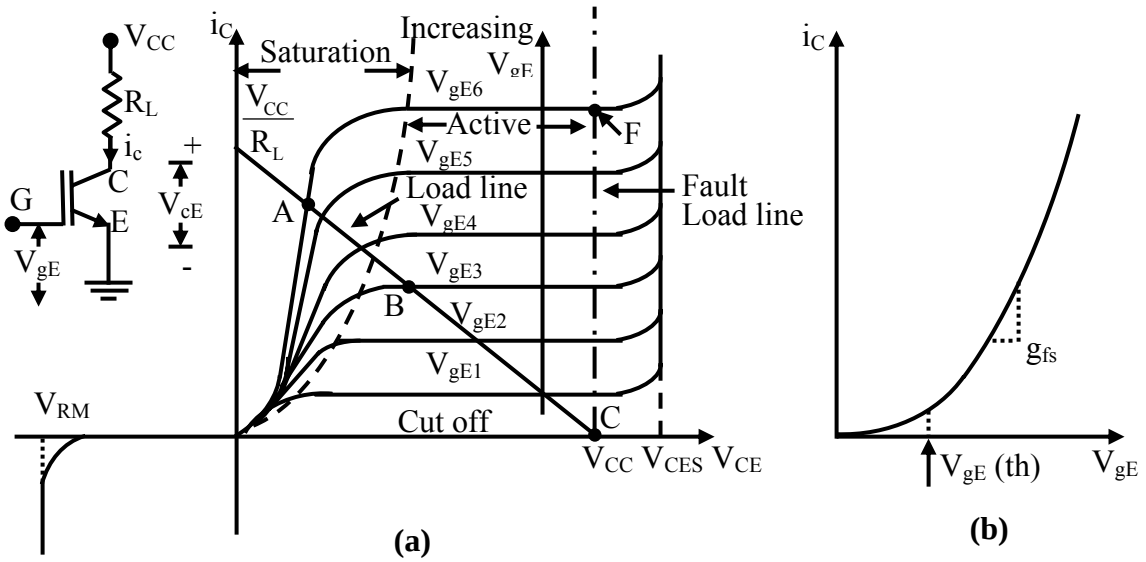



**Fig. 7.4: Static characteristics of an IGBT**
**(a) Output characteristics; (b) Transfer characteristics**

When the gate emitter voltage is below the threshold voltage only a very small leakage current flows though the device while the collector – emitter voltage almost equals the supply voltage (point C in Fig 7.4(a)). The device, under this condition is said to be operating in the cut off region. The maximum forward voltage the device can withstand in this mode (marked $V_{CES}$ in Fig 7.4 (a)) is determined by the avalanche break down voltage of the body – drain **p-n** junction. Unlike a BJT, however, this break down voltage is independent of the collector current as shown in Fig 7.4(a). IGBTs of Non-punch through design can block a maximum reverse voltage ($V_{RM}$) equal to $V_{CES}$ in the cut off mode. However, for Punch Through IGBTs $V_{RM}$ is negligible (only a few tens of volts) due the presence of the heavily doped **n+** drain buffer layer.

As the gate emitter voltage increases beyond the threshold voltage the IGBT enters into the active region of operation. In this mode, the collector current $i_c$ is determined by the transfer characteristics of the device as shown in Fig 7.4(b). This characteristic is qualitatively similar to that of a power MOSFET and is reasonably linear over most of the collector current range. The ratio of $i_c$ to ($V_{gE} - v_{gE(th)}$) is called the forward transconductance ($g_{fs}$) of the device and is an important parameter in the gate drive circuit design. The collector emitter voltage, on the other hand, is determined by the external load line ABC as shown in Fig 7.4(a).

As the gate emitter voltage is increased further $i_c$ also increases and for a given load resistance ($R_L$) $v_{CE}$ decreases. At one point $v_{CE}$ becomes less than vgE – $v_{gE}$(th). Under this condition the driving MOSFET part of the IGBT (Fig 7.2(c)) enters into the ohmic region and drives the output **p-n-p** transistor to saturation. Under this condition the device is said to be in the saturation mode. In the saturation mode the voltage drop across the IGBT remains almost constant reducing only slightly with increasing $v_{gE}$.

In power electronic applications an IGBT is operated either in the cut off or in the saturation region of the output characteristics. Since $v_{CE}$ decreases with increasing $v_{gE,}$ it is desirable to use the maximum permissible value of $v_{gE}$ in the ON state of the device. $v_{gE}$(Max) is limited by the maximum collector current that should be permitted to flow in the IGBT as dictated by the "latch-up" condition discussed earlier. Limiting $V_{gE}$ also helps to limit the fault current through

the device. If a short circuit fault occurs in the load resistance $R_L$ (shown in the inset of Fig 7.4(a)) the fault load line is given by CF. Limiting $v_{gE}$ to $v_{gE6}$ restricts the fault current corresponding to the operating point F. Most IGBTs are designed to with stand this fault current for a few microseconds within which the device must be turned off to prevent destruction of the device.

It is interesting to note that an IGBT does not exibit a BJT-like second break down failure. Since, in an IGBT most of the collector current flows through the drive MOSFET with positive temperature coefficient the effective temperature coefficient of $v_{CE}$ in an IGBT is slightly positive. This helps to prevent second break down failure of the device and also facilitates paralleling of IGBTs.

**Exercise 7.2**

Fill in the blank(s) with the appropriate word(s).

i. From the input side the IGBT behaves essentially as a _____.

ii. When the gate emitter voltage is below _____ no _____ layer is formed in the **p** type body region.

iii. Electrons arriving through the drive MOSFET causes _____ injection from the _____ to the drain drift region.

iv. In an IGBT most of the collector current flows through the _____ and not through the _____.

v. When the gate-emitter voltage of an IGBT is below threshold if operates in the _____ region.

vi. In the active region of operation the collector current of an IGBT is determined by the _____ characteristics which is reasonably _____ over most of the collector current range.

vii. For the same load resistance as the $v_{gE}$ of an IGBT is increased it enters _____ region.

viii. The forward voltage drop of an IGBT in the saturation region remains approximately _____.

ix. An IGBT has small _____ temperature coefficient of on state voltage drop.

x. An IGBT does not exhibit _____ failure mode.

**Answers:**
i) MOSFET; ii) threshold, inversion; iii) hole, collector; iv) MOSFET, BJT; v) cut-off; vi) transfer, linear; vii)saturation; viii) constant; ix) positive; x) second break down.

## 7.5 Switching characteristics of IGBT

Switching characteristics of the IGBT will be analyzed with respect to the clamped inductive switching circuit shown in Fig 7.5(a). The equivalent circuit of the IGBT shown in Fig 7.5 (b) will be used to explain the switching waveforms.

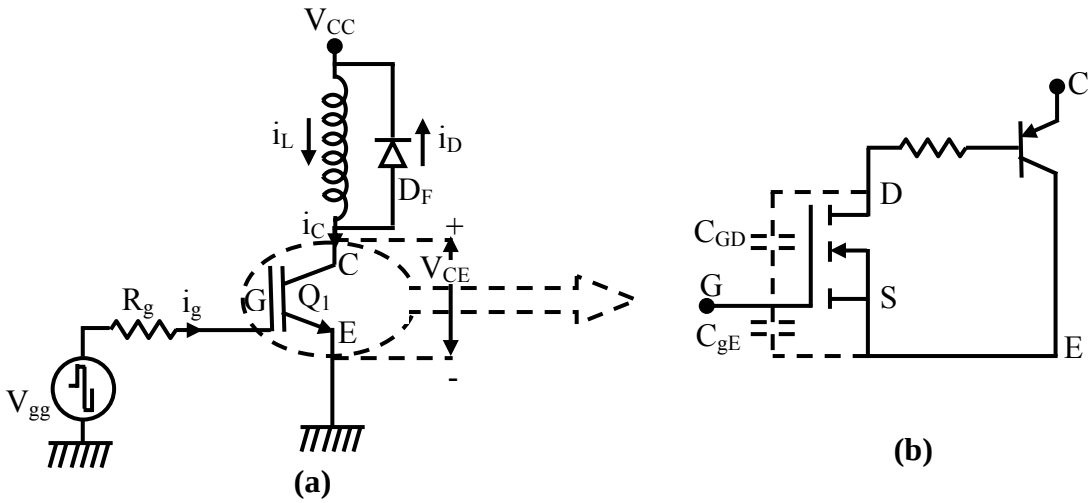



**Fig. 7.5: Inductive switching circuit using an IGBT**
**(a) Switching circuit; (b) Equivalent circuit of the IGBT**

The switching waveforms of an IGBT is, in many respects, similar to that of a Power MOSFET. This is expected, since the input stage of an IGBT is a MOSFET as shown in Fig 7.5(b). Also in a modern IGBT a major portion of the total device current flows through the MOSFET. Therefore, the switching voltage and current waveforms exhibit a strong similarity with those of a MOSFET. However, the output **p-n-p** transistor does have a significant effect on the switching characteristics of the device, particularly during turn off. Another important difference is in the gate drive requirement. To avoid dynamic latch up, (to be discussed later) the gate emitter voltage of an IGBT is maintained at a negative value when the device is off.

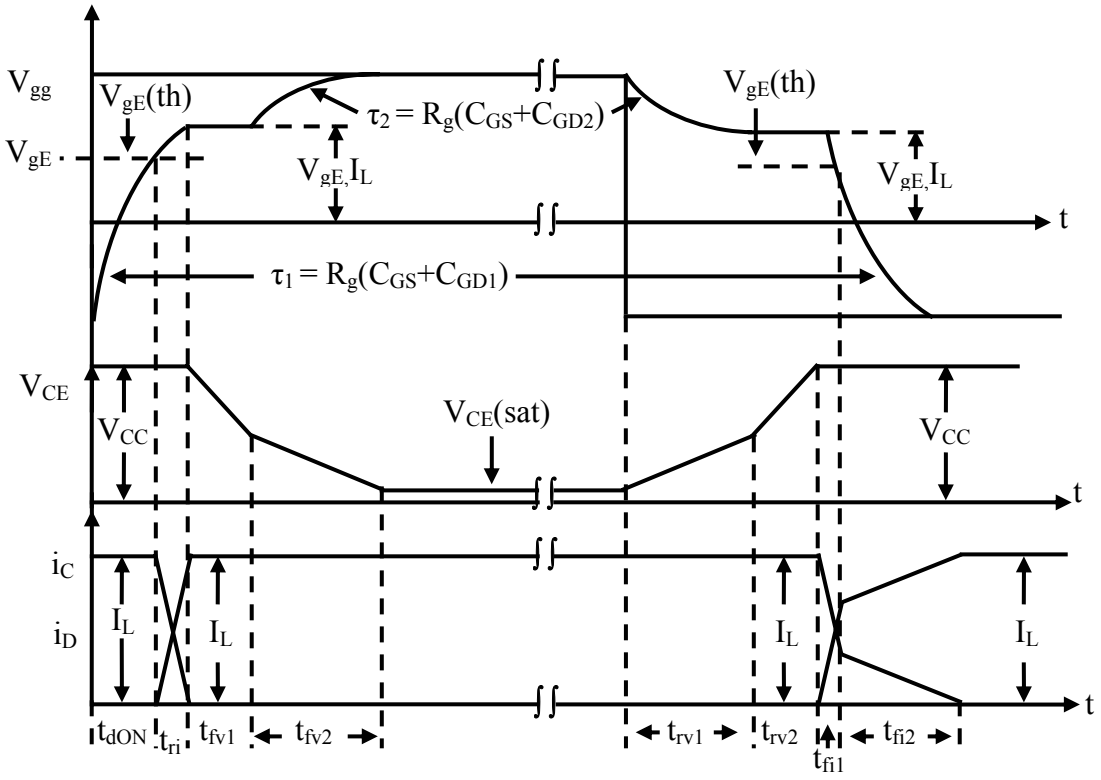



**Fig. 7.6: Switching waveforms of an IGBT.**

The switching waveforms of an IGBT is shown in Fig 7.6. Similarity of these waveforms with those of a MOSFET is obvious. To turn on the IGBT the gate drive voltage changes from $-V_{gg}$ to $+V_{gg}$. The gate emitter voltage $v_{gE}$ follows $V_{gg}$ with a time constant $\tau_1$. Since the drain source voltage of the drive MOSFET is large the gate drain capacitor assumes the lower value $C_{GD1}$. The collector current $i_c$ does not start increasing till $v_{gE}$ reaches the threshold voltage $v_{gE}(th)$. Thereafter, $i_c$ increases following the transfer characteristics of the device till $v_{gE}$ reaches a value $v_{gE}I_L$ corresponding to $i_c = i_L$. This period is called the current rise time $t_{ri}$. The free wheeling diode current falls from $I_L$ to zero during this period. After $i_c$ reaches $I_L$, $v_{gE}$ becomes clamped at $v_{gE}$ $I_L$ similar to a MOSFET. $v_{CE}$ also starts falling during this period. First $v_{CE}$ falls rapidly ($t_{fv1}$) and afterwards the fall of $v_{CE}$ slows down considerably. Two factors contribute to the slowing down of voltage fall. First the gate-drain capacitance $C_{gd}$ will increase in the MOSFET portion of the IGBT at low drain-source voltages. Second, the **pnp** transistor portion of the IGBT traverses the active region to its on state more slowly than the MOSFET portion of the IGBT. Once the **pnp** transistor is fully on after $t_{fv2}$, the on state voltage of the device settles down to $v_{CE}(sat)$. The turn ON process ends here.

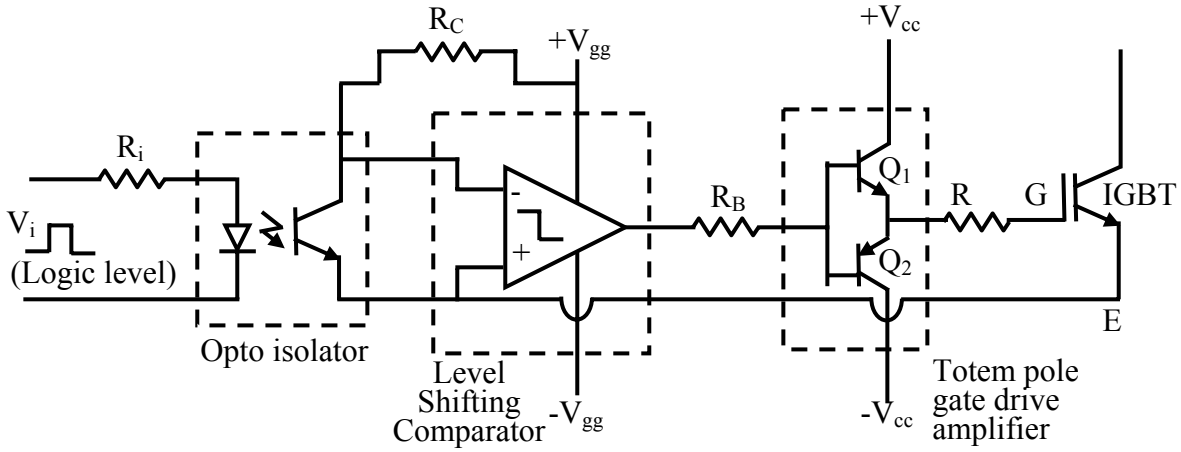
The turn off process of an IGBT follows the inverse sequence of turn ON with one major difference. Once $v_{gE}$ goes below $v_{gE}(th)$ the drive MOSFET of the IGBT equivalent circuit turns off. During this period ($t_{fi1}$) the device current falls rapidly. However, when the drive MOSFET turns off, some amount of current continues of flow through the output **p-n-p** transistor due to stored charge in its base. Since there is no reverse voltage applied to the IGBT terminals that could generate a negative drain current, there is no possibility for removing the stored charge by carrier sweep-out. The only way these excess carriers can be removed is by recombination within the IGBT. During this recombination period ($t_{fi2}$) the remaining current in the IGBT decays relatively slowly forming a current fail. A long $t_{fi2}$ is undesirable, because the power dissipation

in this interval will be large due to full collector-emitter voltage. $t_{fi2}$ can be reduced by decreasing the excess carrier life time in the **p-n-p** transistor base. However, in the process, on state losses will increase. Therefore, judicious design trade offs are made in a practical IGBT to give minimum total loss.

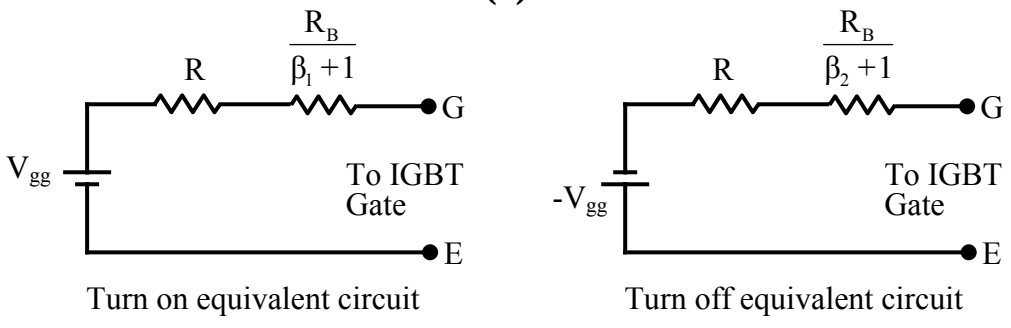
The gate drive circuit of an IGBT should ensure fast and reliable switching of the device. In particular, it should.

- Apply maximum permissible $V_{gE}$ during ON period.
- Apply a negative voltage during off period.
- Control $di_c/dt$ during turn ON and turn off to avoid excessive Electro magnetic interference (EMI).
- Control $dV_{ce}/dt$ during switching to avoid IGBT latch up.
- Minimize switching loss.
- Provide protection against short circuit fault.

Detailed discussion on IGBT gate drive circuit is beyond the scope of this lesson. References [4] & [5] provide good discussion on this subject. Fig 7.7(a) shows a simplified IGBT gate drive circuit.




**(a)**




**(b)**

**Fig. 7.7: IGBT gate drive circuit**
**(a) Gate drive**
**(b) Equivalent circuit of the gate drive during turn on and turn off.**

The logic level gate drive signal is first opto-isolated and fed to a level shifting comparator. This stage converts the unipolar (usually positive) out put voltage of the opto-isolator to a bipolar ($\pm V_{gg}$) signal compatible to the IGBT gate drive levels. The output of the comparator feeds a totem pole output amplifier stage which drives the IGBT. The equivalent circuit of the gate drive during turn on and off are shown in Fig 7.7(b). If $|V_{CC}| > |V_{gg}|$ then both $Q_1$ and $Q_2$ will operate in the active region and reasonably constant value of $\beta_1$ & $\beta_2$ of these two transistors can be used for analysis purpose. These equivalent circuits along with the model of the IGBT input MOSFET can be used to analyze the switching performance of the device. Conversely, for a desired switching performance a suitable gate drive circuit can be designed.

## 7.6 IGBT ratings and safe operating area

**Maximum collector-emitter voltage ($V_{CES}$):** This rating should not be exceeded even on instantaneous basis in order to prevent avalanche break down of the drain-body **p-n** junction. This is specified at a given negative gate emitter voltage or a specified resistance connected between the gate and the emitter.

**Maximum continuous collector current ($I_C$):** This is the maximum current the IGBT can handle on a continuous basis during ON condition. It is specified at a given case temperature with derating curves provided for other case temperatures.

**Maximum pulsed collector current ($I_{CM}$):** This is the maximum collector current that can flow for a specified pulse duration. This current is limited by specifying a maximum gate-emitter voltage.

**Maximum gate-emitter voltage ($V_{gES}$):** This is the maximum allowable magnitude of the gate-emitter voltage (of both positive and negative polarity) in order to

- Prevent break down of the gate oxide insulation.
- Restrict collector current to $I_{CM}$.

**Collector leakage current ($I_{CES}$):** This is the leakage collector current during off state of the device at a given junction temperature. This is usually specified at $V_{gE} = 0V$ and $v_{CE} = V_{CES}$.

**Gate-emitter leakage current ($I_{GES}$):** Usually specified at $v_{CE} = 0V$ & $v_{gE} = v_{gES}$.

**Collector emitter saturation voltage ($V_{CE}(sat)$):** This is specified at a given junction temperature, gate-emitter voltage and collector current. For more detailed data the output characteristics of the device for different $v_{gE}$ and expanded near the saturation zone is also provided.

**Gate-emitter threshold voltage ($v_{gE}(th)$):** It is specified at a low collector emitter voltage and collector current.

**Forward Transconductance ($g_{fs}$):** This is again specified at a low value of $v_{CE}$. For more detailed data the transfer characteristics of the device ($i_c$ $v_s$ $v_{gE}$) is also provided.

**Input, output and transfer capacitances ($C_{ies}$, $C_{oes}$ & $C_{res}$):** These are, gate-emitter, collector-emitter and gate-drain capacitances of the device respectively, specified at a given collector-emitter voltage. Variation of these parameters as functions of $v_{CE}$ are also supplied.

**Switching times ($t_d$(ON) $t_{ri}$, $t_{fv}$, $t_{rv}$, $t_{fi}$):** These times are specified for inductive load switching as functions of gate charging resistance and collector current. In addition turn on and turn off energy losses per switching operation are also specified.

**Maximum total power dissipation ($P_{tmax}$):** This is the maximum allowable power lass in the device (both switching and conduction) on a continuous basis at a given case temperature. Derating curve at other temperatures are also specified.

The IGBT has robust SOA both during turn on and turn off. Fig 7.8 (a) shows the FBSOA. On the left side it is restricted by the forward voltage drop characteristics. Up to maximum continuous collector current this voltage remains reasonably constant at a low value. However, at $I_{CM}$ this voltage starts increasing as the IGBT starts entering active region. On the top the FBSOA is restricted by $I_{CM}$.

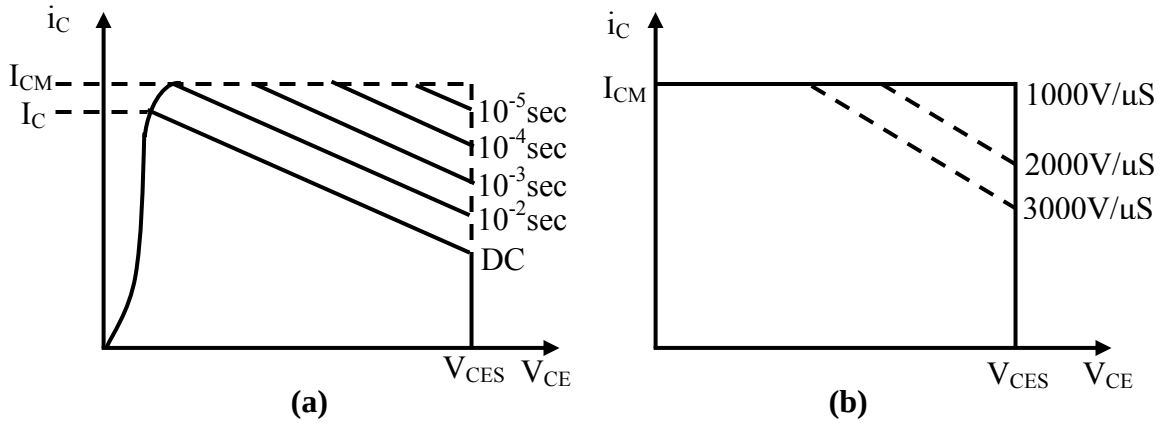



**Fig. 7.8: Safe operating area of an IGBT**
**(a) FBSOA; (b) RBSOA.**

The other two limits are formed by the maximum power dissipation limit and the maximum forward voltage limit. Like other devices the maximum power dissipation limit increases with reduction in the on pulse width.

The RBSOA for low values of $dv_{CE}/dt$ is rectangular. However, for increased $dv_{CE}/dt$ the upper-right hand corner is progressively cut out. The reason for this restriction on the RBSOA is to avoid dynamic latch up. The device user can easily control $dv_{CE}/dt$ by proper choice of $V_{gg}$ and the gate drive resistance.

**Exercise 7.3**

Fill in the blank(s) with the appropriate word(s).

i. In a modern IGBT most of the collector current flows through the _____ and not the _____.

ii. To avoid _____ the gate emitter voltage of an IGBT is maintained at a _____ value when the device is off.

iii. During turn on of an IGBT the rate of fall of voltage slows down towords the end since the output p-n-p transistor traverses its _____ region more _____ compared to the drive MOSFET.

iv. During turn off of an IGBT a _____ is formed due to excess stored charge in the _____ region of the output p-n-p transistor.

v. The gate drive circuit of an IGBT should control $^{dic}/_{dt}$ to avoid excessive _____.

vi. $\frac{dv_{CE}}{dt}$ of an IGBT during turn off should be controlled to prevent _____ of the device.

vii. A specified maximum gate emitter voltage of an IGBT helps to limit the collector current during _____ fault.

viii. Collector emitter saturation voltage of an IGBT _____ with increasing gate-emitter voltage.

ix. The FBSOA of an IGBT is similar to that of a _____ except that the on state voltage drop is much _____.

x. The upper right hand corner of the IGBT RBSOA is gradually cut out with increasing _____ to avoid _____ of the device.

**Answer:** (i) MOSFET, BJT; (ii) latch up, negative; (iii) active, slowly; (iv) current tail, base; (v) EMI; (vi) Latch up; (vii) short circuit; (viii) decreases; (ix) MOSFET, lower; (x) $^{dv_{CE}}/_{dt}$, latch up.

## Reference

[1] B. Jayanta Baliga, "Evolution of MOS Bipolar Power Semiconductor Technology", Proceedings of the IEEE, vol. 76, No. 4, April 1988, pp 409-418.

[2] "Power electronics, Converters, Applications and Design", Mohan, Undeland, Robbins; John Wiley & Sons, 2003

[3] B. Jayanta Baliga et. al, "The Insulated Gate Transistor: A new Three-Terminal MOS-Controlled Bipolar. Power Device", IEEE transaction on Electron Devices, vol. ED-31, No. 6 June 1984 pp 421-828.

[4] Allen R. Hefner, "An Investigation of the drive circuit requirements for the Power Insulated Gate Bipolar Transistor", IEEE Transactions on Power Electronics. Vol. 6 No. 2. April 1991.

[5] Carmelo Licitra et. al, "A New Driving circuit for IGBT Devices", IEEE Transaction on Power Electronics, Vol. 10, No-3 may 1995.

[6] "SEMIKRON Power Electronics News 2001", SEMIKRON International, Germany.

## Lesson Summary

- IGBT is a hybrid device which combines the advantages of MOSFET and BJT.
- An IGBT is formed by adding a **p+** collector layer on the drain drift layer of a Power MOSFET.
- Punch through IGBT has a thin **n+** buffer layer between the **p+** collector layer and **n-** drain drift layer. They have significantly lower conduction loss.
- The IGBT cell structure embeds a parasitic thyristor in it. Latching up of this thyristor is prevented by special structuring of the body region and increasing the effectiveness of the body shorting.
- From the operational point of view an IGBT is a voltage controlled bipolar device.
- The operational equivalent circuit of an IGBT has an **n** channel MOSFET driving a **p-n-p** BJT.
- Like other semiconductor devices on IGBT can also operate in the cut off active and saturation regions.
- When the gate-emitter voltage of an IGBT is below threshold it operates in the cut off region.
- For a given load resistance the operating point of an IGBT can be moved from cut off to saturation through the active region by increasing the gate-emitter voltage.
- In the active region, the collector current of an IGBT is determined by the gate-emitter voltage which can be limited to a given maximum value to limit the fault current through the device in the event of a load short circuit.
- The IGBTs have a slightly positive temperature coefficient of the on-state voltage drop which makes paralleling of these devices simpler.
- An IGBT does not exhibit second break down phenomena as in the case of a BJT.
- The switching characteristics of an IGBT is similar to that of a MOSFET.
- To avoid dynamic latch up of the parasitic thryrstor in an IGBT, the gate emitter voltage of the device is maintained at a negative value during it's off period.
- During turn off, the collector current of an IGBT can exhibit "current tailing" due to stored base change in the base region of the output **p-n-p** transistor.
- The forward bias SOA of an IGBT is similar to that of a MOSFET except the on state voltage drop being much lower.
- The maximum allowable collector current in an IGBT is restricted by the static latch up consideration.

- The RBSOA of an IGBT is rectangular for low values of $\frac{dv_{CE}}{dt}$. For higher $dv_{CE}/dt$ the upper right half corner of the RBSOA is progressively cut-out to prevent "dynamic latch up of the device".
- The IGBT can switch at moderately high frequency (<20 kHZ) and in this range is likely to replace the BJTs in all medium to high power applications.

# Practice Problems and Answers

Q1. What effects do the width and doping level of the drain drift region of an IGBT have on its performance.

Q2. (a) In an IGBT a major portion of the collector current flow through the driver MOSFET section which has a voltage rating almost same as the device. Then how does the on state voltage drop of an IGBT remain low compared to an equivalent MOSFET?

(b) An IGBT is used to switch a resistive load of 5Ω from a DC supply of 350 volts as shown in the inset of Fig 7.4 (a). The ON state gate voltage is $v_{gE}$ = 15v. For the IGBT, $v_{gE}$ (th) = 4 volts and $g_{ts}$ = 25. Find out the maximum current flowing through the IGBT in the event of a short circuit fault across the load. Also find out the power dissipation inside the device.

Q3. What do you under stand by "dynamic latch up" of an IGBT. How can it be prevented?

Q4. What steps are taken in the cell structure design of an IGBT to minimize the "tail current" during turn off operation.

Q5. In the basic gate drive circuit of an IGBT shown in Fig 7.7 (a) following data are given

$V_{gg}$ = 15 V, $V_{cc}$ = 20 V, $\beta_1$ for $Q_1$ = 50, $\beta_2$ for $Q_2$ = 50.

$R_B$ = 2.2 KΩ, R = 30Ω, $V_{gE}$ (th) of IGBT = 4V, $g_{fs}$ = 40

CgE = 4nF, CgD = 500pF,

The IGBT is used to switch a clamed inductive load of 50 Amps from a 400 volts supply.

Find out maximum values of $\left|\frac{dic}{dt}\right|$ and $\left|\frac{dv_{CE}}{dt}\right|$ during Turn on and Turn off of the IGBT.

# Answers to Practice Problems

1. The width and doping level of the drain drift layer of an IGBT affects the performance of the IGBT in several ways.

   - They determine the forward break down voltage of the IGBT.
   - Referring to Fig 7.2 (b), the drain drift region constitutes the base of the upper **p-n-p** transistor. The width and the doping level of this layer determines the current gain "$\propto$" of this transistor. This is intentionally kept low so that most of the device current flows through the MOSFET and not the output **p-n-p** transistor collector. This helps to reduce the voltage drop across the body spreading resistance between the base and emitter of the lower **p-n-p** transistor. Thus the possibility of turning on this transistor and consequent latch up of the device is minimized.
   - Since the major part of the device current flows through the MOSFET which has a positive temperature coefficient of drain source voltage drop, the collector-emitter voltage drop across the device exhibits a slightly positive temperature coefficient. This eliminates the possibility of second break down failure in IGBTs and simplifies paralleling of these devices.

2. (a) The total voltage drop across a conducting IGBT has three components. The voltage drop across the emitter-base junction of the output **p-n-p** transistor follows the usual exponential low of a **p-n** junction. The next component of the voltage drop is due to the drain drift region resistance. In a normal high voltage MOSFET this component of the voltage drop is large due to lower doping level (necessary for blocking high voltage) of this region. However, in a conducting IGBT electrons arriving at the drain drift region through the MOSFET channel causes large minority carrier injection from the **p+** collector. The consequent conductivity modulation reduces the resistance (and hence the voltage drop) in this region. The third component of the IGBT voltage drop occurs across the channel of the driving MOSFET and is same as that of an equivalent high voltage MOSFET. Therefore, the reduced voltage drop across a conducting IGBT is due to reduction of the drain drift region resistance by "conductivity modulation".

   (b) In the event of a short circuit across the load the voltage across the device will be 350 volts and the IGBT will operate in the active region. In this region

$$i_C = g_{fs}\left(v_{gE} - v_{gE}(th)\right)$$

   Substituting the given values

$$i_C\big|_{Max} = 25(15-4) = 275 \text{ Amps}$$

   Power dissipation inside the device will be

$$P_D = v_{CE}\, i_C\big|_{Max} = 350 \times 275 = 96.25 \text{ kW}$$

3. Static latch up in an IGBT occurs when the continuous ON state current exceeds a critical value. However, under dynamic conditions, when the IGBT is switching from on to off state if may latch up at drain current less than this value. During turn off, the voltage across the driver MOSFET increases rapidly. This voltage is blocked by the drain-body **p-n** junction. To block the rapid build up of the voltage the width of the depletion region in the drain drift layer also increases rapidly. This rapid increase in the depletion layer width temporally increases the current gain "$\propto$" of the output **p-n-p** transistor and causes latch up of the device at a lower collector current than would have been necessary for static latch up.

4. Punch Through and Non-punch through IGBTs solve the problem of tail current by two different approaches. Punch through IGBT s attempt to minimize the current tailing problem by shortening the duration of the tailing time. This is done by reducing the excess carrier life time in the **n+** buffer layer compared to the n- drain drift layer. This n+ buffer layer acts as a sink for excess holes and greatly enhances the removal rate of holes from the drain drift layer. Thus the tail time is reduced.

   Non punch through IGBTs attack the current tailing problem by minimizing the magnitude of the current during the failing interval. This is done by designing the IGBT so that the MOSFET section carries as much of the total current as possible. Newer NPT IGBT designs have more than 90% of the total current carried by the MOSFET section of the device.

5. During turn on and turn off the IGBT passes through the active region.

   When $v_{gE}$ is greater than $v_{gE}(th)$ the collector current is given by

$$i_C = g_{fs}\left(v_{gE} - v_{gE}(th)\right)$$

$$\therefore \frac{dic}{dt} = g_{fs}\frac{d}{dt}v_{gE}$$

   But from the equivalent circuit of the IGBT gate drive circuit during turn on

$$\frac{d}{dt}v_{gE} = \frac{V_{gg} - v_{gE}}{\left(C_{gE} + C_{gD}\right)\left(R + \frac{R_B}{\beta_1 + 1}\right)}$$

$$\therefore \frac{dic}{dt} = g_{fs}\frac{d}{dt}v_{gE} = \frac{g_{fs}\left(V_{gg} - v_{gE}\right)}{\left(C_{gE} + C_{gD}\right)\left(R + \frac{R_B}{\beta_1 + 1}\right)}$$

   In the active region $V_{gg} >> v_{gE}$

   Also since $V_{cc} > V_{gg}$, $Q_1$ & $Q_2$ operates in the active region.

   Substituting the given values

$$\frac{dic}{dt} = \frac{40 \times 15}{4500 \times 10^{-12} \times \left(30 + \frac{2200}{51}\right)} = 1.82 \times 10^{9} \text{ A/Sec}$$

Since $\beta_1 = \beta_2$ , $\frac{dic}{dt}$ during turn off will also have the same value

$$\text{So } \left|\frac{dic}{dt}\right| = 1.82 \text{ A/ns}$$

Since load current is 50 Amps and $g_{fs} = 40$

$$v_{ge}\, I_L = v_{gE}(th) + \frac{I_L}{g_{fs}} = 5.25 \text{ volts}$$

Daring turn on $C_{gD} \frac{dv_{CE}}{dt} = i_g\, I_L = \frac{V_{gg} - v_{gE}\, I_L}{R + \frac{R_B}{\beta+1}}$

$\therefore$ $\frac{dv_{CE}}{dt}$ during turn ON is

$$\frac{dv_{CE}}{dt} = \frac{V_{gg} - v_{gE}\, I_L}{C_{gD}\left(R + \frac{R_B}{\beta_1+1}\right)} = \frac{15 - 5.25}{500 \times 10^{-12}\ \left(30 + \frac{2200}{51}\right)}$$

$$= 2.67 \times 10^{8} \text{ V/Sec}$$

Since $V_{gg+} = V_{gg-}$ and $\beta_1 = \beta_2$

$\frac{dv_{CE}}{dt}$ during turn off will be same

So $\left|\frac{dv_{CE}}{dt}\right| = 2.67 \times 10^{8}$ V/Sec or 267 V/μs.