METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTORS (MOSFETs)

Principle of Operation

A four-terminal device obtained from an extension of the two-terminal MIS structure by diffusing or implanting two n+ regions into the p-type substrate in order to form two ohmic contacts called the source and the drain.

A thin layer SiO₂ separates the third contact (gate) from the channel region of the device, and a fourth contact (body or bulk or substrate) is connected to the substrate.

When a positive voltage is applied to the gate, a thin channel of electrons is created near the Si- SiO₂ interface, which provides a conducting link between the source and the drain => on state of the device.

In the absence of a conducting channel, no electrical continuity between the drain and the source exists => off state of the device.

The depletion regions between the p-type substrate and n+ regions and n-channel provide the required isolation from other devices fabricated on the same substrate.

In the on state of the device, an applied drain-to-source bias creates a drift field in the channel, and electrons move from the source to the drain => thus a current is established.
The electron concentration in the channel (and, thus, the channel conductance and device current) can be modulated by a variation in the gate voltage.

**Note:** the C-V characteristic of this device shows low-frequency behavior (of the two-terminal MIS structure) up to a fairly high frequency (of the order of the inverse transit time of the carriers across the channel), since the heavily doped source/drain regions provide an infinite reservoir, from which the carriers can move into the channel, or to which they can escape from the channel.

**The I-V Characteristic**

**The Gradual Channel Approximation (GCA)**

- The GCA, proposed by Shockley, is used in order to calculate the I-V characteristic of the device.
- This approximation states that the rate of variation of the lateral field within the channel is much smaller than the rate of variation of the vertical field, i.e., \( \left| \frac{\partial F_x}{\partial x} \right| \ll \left| \frac{\partial F_y}{\partial y} \right| \), and the channel potential is assumed to be a gradually changing function of position.

**Note:** This approximation actually states that the channel potential varies very little along the channel over a distance of the order of the insulator thickness \( d_i \), i.e., this requires \( d_i \ll L \), where \( L \) is the channel length.

- The gradual channel approximation (GCA):
  - Fig (a) schematic comparison of the parallel \( F_{||} \) and perpendicular \( F_{\perp} \) electric fields in the channel, and
  - Fig (b) qualitative potential profile in the channel.
However, modern MOSFETs have extremely short channel lengths, and this requirement is not often met; thus, the GCA fails for most of modern MOSFETs, nevertheless its discussion is important.

According to GCA, the charge induced at any position along the channel can be determined from the formulas derived for the MIS structure, provided the constant surface potential $V_s$ for an MIS structure is replaced by a variable channel potential $V_c(x)$ in the expression for the surface charge density per unit area $Q'_s$ in the semiconductor.

**Assumption:** The device is operating in the above threshold regime, i.e., the gate voltage is sufficiently large to create strong inversion throughout the channel.

The induced surface charge density $Q'_s$ is then given by

$$Q'_s = -C'_f[V_g - V_F - 2\phi_b - V_c(x)] \tag{5.1}$$

where $C'_f$ is the insulator capacitance per unit area, and the term within the square brackets is the voltage drop across the insulator.

**Note:** here we are considering an n-channel device, however, all the results are also applicable for a p-channel device, provided appropriate sign changes are made.

Band diagrams at

Fig (a) the source side and
Fig (b) the drain side of the channel for the direction perpendicular to the Si-\(\text{SiO}_2\) interface.
Assume that the source is grounded \([\text{i.e., } V_s(0) = 0]\), the drain is connected to a potential \(V_D \text{ [i.e., } V_s(L) = V_D]\), and the substrate is connected to the source \([\text{i.e., } V_{sub} = 0]\).

The density of the free electrons \(n_s\) in the channel can be found from the difference between the total surface charge density \(Q'_s\) and the depletion charge density \(Q'_{dep}\), i.e.,

\[
n_s = \frac{1}{q} \left[ V_g - V_{FB} - 2\Phi_b - V_c(x) - Q'_s \right] \tag{5.2}
\]

Note: at the source side of the gate where \(V_c = 0\), \(Q'_{dep}\) is given by

\[
Q'_{dep} = -qN_A d_{dep} = -\sqrt{4q\varepsilon_s N_A \Phi_b} \tag{5.3}
\]

however, elsewhere in the channel, the total band bending between the substrate and the surface is \(2\Phi_b + V_c(x)\), since the induced n-channel/p-substrate junction is reverse biased by the \(V_c(x)\).

The band bending increases in the channel as one moves from the source to the drain, which leads to an increase in the width of the depletion layer and of the depletion charge density, thus, the exact expression for \(Q'_{dep}\) can be given by

\[
Q'_{dep}(x) = -qN_A d_{dep}(x) = -\sqrt{2q\varepsilon_s N_A [2\Phi_b + V_c(x)]} \tag{5.4}
\]

Since the drain current \(I_D\) is carried entirely due to drift, its expression can be given by

\[
I_D = q\mu_n n_s W \frac{dV_c(x)}{dx} \tag{5.5}
\]

where \(\mu_n\) is the low-field electron mobility, and \(W\) is the channel width.
In writing this equation, it is assumed that the electron drift velocity $v_n$ is proportional to the component of the electric field parallel to the Si-SiO$_2$ interface, i.e., $v_n = \mu_n F_{||}$.

**Note:** for short channel devices, this electric field may be sufficiently high to cause velocity saturation in the channel.

Thus, the drain current equation can be rewritten as

$$\frac{dI}{dx} = \frac{q \mu_n W n_s}{I_D} dV_o$$

(Note: $n_s$ is a function of $V_b$; thus, substituting the expression for $n_s$ in the above equation, noting that $I_b$ is a constant throughout the channel, and integrating it from the source, i.e., $x = 0$ ($V_b = 0$) to the drain, i.e., $x = L$ ($V_b = V_D$), the following I-V characteristic is obtained:

$$I_D = \mu_n C_i^f \frac{W}{L} \left[ \left( V_g - V_{FB} - 2q \phi_b - \frac{V_D}{2} \right) V_0 - \frac{2}{3} \sqrt{2q \varepsilon_s N_A} \left( V_D + 2q \phi_b \right)^{3/2} (2q \phi_b)^{3/2} \right]$$

(5.7)

- This model is known as the Shockley model.
- This expression for $I_b$ is valid only if the inversion layer exists even at the drain side of the gate, i.e., $n_s(L) \geq 0$.
- The condition $n_s(L) = 0$ is referred to as the pinch-off condition, and it occurs at the drain side of the gate when

$$V_D = V_{Dsat} = V_g - V_{FB} - 2q \phi_b + \frac{q \varepsilon_s N_A}{C_i^f} \left[ 1 + \left\{ 1 + \frac{2(V_g - V_{FB})C_i^f}{q \varepsilon_s N_A} \right\}^{1/2} \right]$$

(5.8)

- As $V_g \rightarrow V_T$, $V_{Dsat} \rightarrow V_g - V_T$ (first-order approximation), where $V_T$ is the threshold voltage corresponding to the onset of strong inversion, and is given by

$$V_T = V_{FB} + 2q \phi_b + \frac{2 \sqrt{2q \varepsilon_s N_A \phi_b}}{C_i^f}$$

(5.9)

- In the presence of a substrate bias $V_{sub}$, the expression for $V_T$ gets modified to

$$V_T = V_{FB} + 2q \phi_b + \frac{2 \sqrt{q \varepsilon_s N_A (2q \phi_b - V_{sub})}}{C_i^f}$$

(5.10)
The band diagram of an n-channel MOSFET along the direction perpendicular to the Si-
SiO₂ interface for a negative substrate bias.

**Note:** \( V_{\text{sub}} \) is the voltage difference between the inversion layer at the source end and the
substrate contact, and its sign should be such that it never forward biases the inversion
layer-substrate junction (a small forward bias, much less than \( 2\Phi_b \) may be allowed in
certain cases).

- If the inversion layer-substrate (or the source-substrate or the drain-substrate) junction
ever gets forward bias, a large leakage current would result, which would hamper normal
MOSFET operation.
- For both n- and p-channel MOSFETs, the magnitude of the threshold voltage \( V_T \)
increases with an increase in \(|V_{\text{sub}}|\).

**Physical Understanding of Saturation**

- A physical insight into the phenomenon of saturation may be obtained by analyzing the
electric field distribution under the gate.
- Integrating Eq.(5.6) from 0 to \( x \), one gets:
\( x = \mu_n W q \int_0^{V_c(x)} \frac{n_s(V')}{I_D} dV' \)

or

\[
x = \frac{\mu_n W C_i'}{I_D} \left[ \left( V_g - V_{FB} - 2\Phi_b - \frac{V_c(x)}{2} \right) V_c(x) \right. \\
- \left. \frac{2}{3} \frac{\sqrt{2} q e s N_A}{C_i'} \left( V_c(x) + 2\Phi_b \right)^{3/2} - (2\Phi_b)^{3/2} \right]
\]

- The electric field \( F = -\frac{dV_c(x)}{dx} \) in the channel in the direction parallel to the semiconductor-insulator interface can be found from Eq.(5.5)

\[
|F| = \frac{I_D}{q \mu_n n_s(V_c) W}
\]

- Solving Eqs.(5.12) and (5.13) together, the field profiles can be calculated.

Fig.5.6 The variation of the electric field along the channel for drain voltage nearly equal to the saturation voltage for gate voltages \( V_{g1} \) (curve 1) and \( V_{g2} \) (curve 2), with \( V_{g2} > V_{g1} \).

- Note: from the constancy of the drain current \( I_D \) throughout the device, it can be seen that as \( V_c(L) \rightarrow V_{DSS}, n_s(L) \rightarrow 0 \) and the electric field \( F(L) \) diverges.
• The differential drain conductance

\[ g_{ds} = \left. \frac{\partial I_D}{\partial V_D} \right|_{V_D = \text{constant}} \quad (5.14) \]

tends to zero when \( V_D \to V_{D\text{sat}} \), and the I-V characteristics may be extrapolated in the voltage region \( V_D > V_{D\text{sat}} \) assuming a constant (independent of \( V_D \)) drain current \( I_{D\text{sat}} \).

• \( I_{D\text{sat}} \) may be found by substituting \( V_D = V_{D\text{sat}} \) from Eq.(5.8) into Eq.(5.7), which results in a highly complicated expression, however, it can be simplified for gate voltages close to the threshold voltage (when \( V_{D\text{sat}} = V_g - V_T \)):

\[
I_{D\text{sat}} = \mu_n C_W \frac{W}{L} \left[ \left( \frac{V_g}{2} - V_{F_b} - 2\phi_b - \frac{V_T}{2} \right) \left( V_g - V_T \right) \right]
- \frac{2}{3} \sqrt{2q_e \frac{N_A}{C'_f}} \left| V_g - V_T + 2\phi_b \right|^{3/2} - \left| 2\phi_b \right|^{3/2} \quad (5.15)
\]

• Note: this approach is only valid when the channel electrons do not suffer any velocity saturation due to high electric fields.

• Note: modern day MOSFETs have extremely small gate lengths, and the channel has high electric fields (more than the critical electric field required for velocity saturation), which creates the velocity saturation effects for the channel electrons.
For very small $V_D$, the terms under the curly brackets in Eq.(5.15) can be expanded in Taylor series, leading to the following simplified expression for the I-V characteristics in the linear region:
A physical justification of Eq.(5.16) can be given as follows:

At very small $V_D$, the charge induced in the channel is, to the first order, independent of the channel potential, thus,

$$q\eta_z = C_i'(V_g - V_T)$$  \hspace{1cm} (5.17)

Now, for small $V_D$, the electric field $F$ in the channel is nearly constant, and is given by $F \approx V_D/L$.

The drain current is entirely due to drift, and is given by the electrons in transit model:

$$I_D = q\eta_z V_h = \mu_n C_i' \frac{W}{L} (V_g - V_T)V_D$$  \hspace{1cm} (5.18)

since $V_h = \mu_n F$

5.2.3 The Charge Control Model

A simplified description of the I-V characteristics of a MOSFET can be obtained by using the charge control model.

In this model, it is assumed that the concentration of free carriers induced in the channel is given by

$$n_z = \frac{C_i'(V_g - V_T - V_c)}{q}$$  \hspace{1cm} (6.19)

Compare Eq.(5.19) with Eq.(5.2): in Eq.(5.19), the variation of the depletion charge density $\phi_{def}'$ with the channel potential has been neglected.

The drain current $I_D$ can now be given by

$$I_D = \mu_n C_i' W (V_g - V_T - V_c) \frac{dV_c}{dx}$$  \hspace{1cm} (5.20)

Compare Eq.(5.20) with Eq.(5.5).

Equation (5.20) can be rewritten as

$$dx = \frac{\mu_n C_i' W (V_g - V_T - V_c)}{I_D} dV_c$$  \hspace{1cm} (5.21)
Integrating Eq.(5.21) from $x = 0$ (source side) to $x = L$ (drain side), which corresponds to a change in $V_G$ from $0$ (at $x = 0$) to $V_D$ (at $x = L$), the following expressions for the I-V characteristics are obtained:

\[
I_D = \frac{\mu_n C_i W}{L} \left[ (V_G - V_T) \frac{V_D}{2} - \frac{V_D^2}{2} \right] \quad \text{for } V_D \leq V_{DSat} \tag{5.22}
\]

and

\[
I_D = \frac{\mu_n C_i W}{2L} (V_G - V_T)^2 \quad \text{for } V_D > V_{DSat} \tag{5.23}
\]

where $V_{DSat} = V_D - V_T$.

Fig. 5.9 The I-V characteristics of an n-channel MOSFET calculated using the charge control model (solid curve) and the Shockley model (dashed curve).

The differential transconductance $g_m$ is defined as

\[
g_m = \left. \frac{\partial I_D}{\partial V_G} \right|_{V_G = \text{constant}} \tag{5.24}
\]

From Eqs.(5.22) and (5.23),
where \( k_N = k'_N \frac{W}{L} \) is referred to as the device transconductance parameter, with \( k'_N = \mu_N C'_1 \) is referred to as the process transconductance parameter.

Thus, in order to achieve a high value for the transconductance \( g_m \), the following steps may be taken.

- Higher value of low field electron mobility \( \mu_N \).
- Thinner gate dielectric layers, which in turn gives large values for the insulator capacitance per unit area \( C'_1 \), since \( C'_1 = \frac{s}{d_i} \).
- Large widths (W) and short lengths (L).
- Note: for short channel devices, where velocity saturation effects are important, the dependence of transconductance on the low-field electron mobility and the gate length gets strongly affected.

**EXAMPLE 5.1**: An n-channel MOSFET with the process transconductance parameter \( k'_N = 40 \, \mu A/V^2 \), the threshold voltage \( V_T = 0.7 \, V \), and \( (W/L) = 10 \) is biased at \( V_G = 1 \, V \). Determine the drain current \( I_D \), the transconductance \( g_m \), and the drain conductance \( g_d \) for i) \( V_D = 0.1 \, V \), and ii) \( V_D = 1 \, V \). Assume \( V_S = V_{SUB} = 0 \).

**SOLUTION:**

i) \( V_G - V_T = 1 - 0.7 = 0.3 \, V \), and \( V_D = 0.1 \, V \), therefore, \( V_D < (V_G - V_T) \);
Hence, the device is under linear mode of operation.

The drain current \( I_D \) = \( k_N \frac{W}{L} \left( V_G - V_T - \frac{V_D}{2} \right) \)

\[ = 40 \times 10^{-6} \times 10 \times \left( (1 - 0.7) \times 0.1 - \frac{0.1^2}{2} \right) \]

\[ = 10 \ \mu A. \]

Transconductance \( g_m = \frac{\partial I_D}{\partial V_G} = k_N \frac{W}{L} V_D = 40 \times 10^{-6} \times 10 \times 0.1 \)

\[ = 40 \ \mu A/V. \]

Drain Conductance \( g_d = \frac{\partial I_D}{\partial V_D} = k_N \frac{W}{L} (V_G - V_T - V_D) \)

\[ = 40 \times 10^{-6} \times 10 \times (1 - 0.7 - 0.1) = 80 \ \mu A/V. \]

Note the huge change in transconductance in saturation as compared to the linear region: this is due to the square law dependence of current on the gate voltage in the saturation region (as against the linear variation in the linear region).

\[ g_d = \frac{\partial I_D}{\partial V_D} = 0! \]

Drain Conductance

This is due to the independence of the saturation drain current on the drain voltage. In reality, channel length modulation creates a change in drain current with respect to the drain voltage in saturation, and finite drain conductance (and output resistance \( r_0 \), given by \( r_0 = 1/g_d \)) results.

**Effect of Source and Drain Series Resistance**

- The analysis so far neglects the effects of the source/drain series resistance, and the entire voltage is assumed to drop along the channel.
- However, for modern day MOSFETs, this effect cannot be ignored, due to smaller diffusion cross-sections and smaller drain currents.
- The extrinsic (measured) voltages \( V_{as} \) and \( V_{ds} \) can be related to the intrinsic (device) voltages \( V_G \) and \( V_B \) by the following equations:
where $R_s$ and $R_d$ are the source and drain resistances respectively.

- The extrinsic transconductance $g_m (= \partial I_D/\partial V_{DS})$ is related to the intrinsic transconductance $g_{m0} (= \partial I_D/\partial V_A)$ by
  
  $$g_m = \frac{g_{m0}}{1 + g_{m0}R_s + g_{d0}(R_s + R_d)}$$

  (5.29)

  where $g_{d0} (= \partial I_D/\partial V_D)$ is the intrinsic drain conductance.

- Similarly, the extrinsic drain conductance $g_d (= \partial I_D/\partial V_DS)$ is related to the intrinsic drain conductance $g_{d0}$ by
  
  $$g_d = \frac{g_{d0}}{1 + g_{d0}(R_s + R_d) + g_{me}R_s}$$

  (5.30)
Fig. 5.10 The variation of the drain saturation current as a function of the gate voltage for three different values of the series source resistance $R_s (= 0 \, \Omega, 100 \, \Omega, \text{and} \, 300 \, \Omega)$.

![Figure 5.10](image)

Fig. 5.11 The drain current drain-to-source voltage characteristics for different values of $V_g$ for: (i) $R_s = R_d = 0 \, \Omega$ (dashed curves) and (ii) $R_s = R_d = 300 \, \Omega$ (solid curves).

- The series source resistance reduces the drain current, and the series drain resistance increases the drain-to-source saturation voltage.
- Both series source resistance and series drain resistance reduce the drain conductance at low drain-to-source voltages.

**Velocity Saturation Effects in MOSFETs**

- In modern day MOSFETs, the channel length is very small, the electric field in the channel is very high, and the velocity saturation effects are very important.
- The measured electron and hole mobilities in the inversion layer may be quite different than those measured in the bulk.
- Note: the channel, in reality, is under a two-dimensional electric field, one directed longitudinally $(F_y)$ from the gate to the substrate, and the other directed laterally $(F_x)$ along the length of the channel.
- The effective inversion layer thickness $d_{eh}$ is approximately given by $d_{eh} \approx \frac{kT}{qF_y}$; thus, a large vertical field creates a narrow inversion layer, and vice versa.
The random path of electrons in the channel, undergoing surface scattering, which is more intense in narrow channels.

- Electrons in the channel move in random directions, undergoing surface scattering, which increases for narrow channels (i.e., under high vertical field $F_y$), thus their mobility drops.

The variation of the electron and hole mobilities in the channel as a function of the gate electric field.

- The dependence of the electron and hole mobilities on the gate field $F_g$ can be crudely approximated by

$$
\mu_n(F_g) = \mu_{n0}/(1 + \alpha_{nn} F_g)^{1/2} \quad \text{and} \quad \mu_p(F_g) = \mu_{p0}/(1 + \alpha_{pp} F_g)^{1/2}
$$

(5.31)

where $n_0$ and $p_0$ are the electron and hole mobilities for $F_g = 0$, $\alpha_{nn} = 1.54 \times 10^{-6} \text{ cm/V}$, and $\alpha_{pp} = 5.35 \times 10^{-6} \text{ cm/V}$. 

• It is very interesting to note that in highly constricted channels or at low temperatures, the carrier mobility is seen to get enhanced.
• This is because for these cases, the electron motion in the direction perpendicular to the Si-SiO₂ interface gets quantized, and the channel electrons behave like a two-dimensional electron gas (2DEG).
• Thus, the surface scattering is not that important, and the impurity scattering is screened by a high density of electrons in the channel.
• Such enhancement of electron mobility was observed in GaAs, and is exploited in high electron mobility transistors (HEMTs) or modulation-doped field effect transistors (MODFETs).

**Effects of Velocity Saturation on the I-V Characteristic**

• For this derivation, a simple two-piece linear approximation for the electron velocity is used:

\[
\begin{align*}
\nu_b &= \mu_e F \quad \text{for } F < F_s \\
&\text{and} \\
\nu_b &= \mu_e F_s = \nu_s \quad \text{for } F \geq F_s 
\end{align*}
\] (5.32)

where \( F_s \) is the electric field required for velocity saturation, and \( \nu_s \) is the saturation limited thermal velocity.

• Recall: in the linear region, the I-V characteristic can be given by:

\[
I_D = k_N(\nu_{gt}V_D - \nu_D^2 / 2)
\] (6.34)

where \( \nu_{gt} = \nu_g - \nu_T \).

• The saturation current \( I_{DSat} \) can now be found by assuming that the current saturation occurs when the electric field at the drain side of the channel exceeds the critical field \( F_s (= \nu_s/\mu_e) \) required for velocity saturation.
• This is a much more realistic assumption than the Shockley model, which assumes saturation occurs when \( n_s(L) \to 0 \), which, in turn, implies \( F(L) \to \infty \).
• The constant mobility model is still used for drain voltages below the saturation voltage.
• The absolute value of the electric field in the channel \( F(x) = |F(x)| = d\nu_c(x)/dx \) at drain voltages below the saturation voltage can be obtained from Eq.(5.21):

\[
F(x) = \frac{I_D}{k_N(\nu_{gt} - \nu_c(x))}
\] (5.35)
Integrating Eq.(5.35) from 0 to \(x\), the following equation for the channel potential \(V_c(x)\) is obtained for drain voltages below the saturation voltage:

\[
x = \frac{k_N L (V_{gt} V_c(x) - V_c(x)^2 / 2)}{I_D} \tag{5.36}
\]

The solution of this equation is given by

\[
V_c(x) = V_{gt} - \left[ \frac{V^2_{gt} - 2I_D x}{k_N L} \right]^{1/2} \tag{5.37}
\]

Substituting Eq.(5.37) into Eq.(5.35), the following expression for the electric field as a function of distance is obtained:

\[
F(x) = \frac{I_D}{k_N L \left( V^2_{gt} - \frac{2I_D x}{k_N} \right)^{1/2}} \tag{5.38}
\]

and the electric field \(F(L)\) at the drain side of the channel (where it is the largest),

\[
F(L) = \frac{I_D}{k_N L \left( V^2_{gt} - \frac{2I_D}{k_N} \right)^{1/2}} \tag{5.39}
\]

From the condition \(F(L) = F_s\), the drain saturation current can now be found as

\[
I_{D_{sat}} = k_N V_{s1} \left[ 1 + \left( \frac{V_{gt}}{V_{s1}} \right)^2 \right]^{1/2} - k_N V_{s1}^2 \tag{5.40}
\]

and the drain saturation voltage

\[
V_{D_{sat}} = V_{gt} + V_{s1} - \left( V_{gt}^2 + V_{s1}^2 \right)^{1/2} \tag{5.41}
\]

where \(V_{s1} = F_s L\).

At very large values of \(V_{s1} (= V_L/\mu_h >> V_{gt})\), the term in the brackets in Eq.(5.40) may be expanded into Taylor series, which gives the following expression for the saturation drain current for long channel devices:

\[
I_{D_{sat}} = k_N V_{gt}^2 / 2, \tag{5.40}
\]

which does not take into account the velocity saturation effects.
• For long channel devices, $V_{s1} \gg V_{g}$, and $V_{Dsat} \rightarrow V_{sat}$, as predicted by the constant mobility model, hence, the velocity saturation effects are not too important for long channel devices.

• Example: assume $V_{g} \approx 3 \text{ V}$, $\mu_n \approx 800 \text{ cm}^2/\text{V-s} \text{ cm}$, and $v_{s} \approx 10^6 \text{ m/s}$, then for channel length $L \gg 2.4 \mu\text{m}$, velocity saturation effects on the drain saturation current may be neglected.

• However, for modern day MOSFETs, the typical gate length is much smaller than $1 \mu\text{m}$, (recently, Intel has introduced processors using $0.15 \mu\text{m}$ technology), where the velocity saturation effects are extremely important.

• In the limiting case for short channel devices, when $V_{s1} \approx 3 \text{ V}$, $\mu_n \approx 800 \text{ cm}^2/\text{V-s} \text{ cm}$, and $v_{s} \approx 10^6 \text{ m/s}$, then for channel length $L \ll 2.4 \mu\text{m}$, velocity saturation effects on the drain saturation current may be neglected.

• Note: for short channel device, the drain saturation current is $2V_{s1}V_{g}$ times smaller than the value predicted by the constant mobility model; and it becomes linearly dependent on $V_{g}$ instead of the familiar square law relation.

• While plotted as a function of $V_{g}$ for a long channel device, shows a linear behavior; however, for short channel devices, it shows a significant departure from linearity a measure of whether the device is a short-channel or a long-channel device.

• The drain saturation voltage is also much smaller than that predicted by the constant mobility model.

![Fig.5.14 The variation of the drain saturation current as a function of the gate length for three different values of the gate voltage (3 V, 5 V, and 7 V). The drain saturation current predicted by the constant mobility model (shown by the dashed line) is also shown for comparison.](image-url)
• The effects of source/drain series resistance, for these cases, can be accounted for (as done earlier for long channel devices), and the following expressions for the drain saturation current and the drain saturation voltage are obtained:

\[
I_{\text{Dsat}} = k_N V_{g}^2 \frac{1 + 2 k_N R_s V_{gst} + \frac{V_{gst}^2}{V_{s1}^2}}{1 - k_N R_s V_{gst}} \left(1 - k_N R_s V_{gst}\right) \frac{1}{2}
\]

(5.42)

and

\[
V_{\text{Dsat}} = V_{gs} + V_{s1} - \left(V_{gs}^2 + V_{s1}^2\right)^{1/2} + I_{\text{Dsat}} (R_s + R_G)
\]

(5.43)

where \(V_{\text{GST}} = V_{gs} - V_T\).

**Interpolated Relation**

• The following interpolation formula for the MOSFET I-V characteristic has been proposed by Shur, which describes both limiting cases (small \(V_D\) \(<< V_{\text{Dsat}}\) and large \(V_D \gg V_{\text{Dsat}}\)) correctly:

\[
I_D = I_{\text{Dsat}} \tanh \left(\frac{g_d V_{ds}}{I_{\text{Dsat}}}\right)
\]

(5.44)

• This was one of the earlier formulas, and a huge amount of work has been done in this area for the last ten years or so, in order to further refine the description of the behavior of short-channel MOSFETs.
• In practical devices, the I-V characteristics do not completely saturate at large drain-to-source voltages, and this is related to the short channel and other nonideal effects in MOSFETs.
• In order to account for the finite slope of the output characteristics in saturation, the following modification to the drain current expression has been proposed:

\[
I_D = I_{\text{Dsat}} \tanh \left[\frac{g_d V_{ds}}{I_{\text{Dsat}}} \left(1 + \lambda V_{ds}\right)\right]
\]

(5.45)

where \(\lambda\) is referred to as the channel-length modulation parameter (an extremely important parameter for short channel device a measure of the nonidealities present in the device)

**Short Channel and Nonideal Effects in MOSFETs**

• For long channel devices, the drain current becomes constant in saturation, whereas, for short channel devices, the drain current increases continuously with the drain-to-source voltage.
Another interesting feature seen in short channel devices is that the saturation current increases as the device length is reduced.

Now, based on the existing model for the threshold voltage, which states that it is independent of the device length this behavior cannot be explained.

In reality, it has been shown that the threshold voltage is a strong function of the channel length (for short channel devices), and it actually decreases with a decrease in the channel length, which explains the reason behind the larger saturation current.

**The Charge Sharing Model**
• The reduction of the threshold voltage with a reduction in the channel length can be explained by the charge sharing model.

Fig.5.17 The depletion charge profiles for (a) a long channel device, and (b) a short channel device.

- For a long channel device, the depletion layer thickness $d_{sd}$ at the source end of the channel and $d_{dd}$ at the drain end of the channel are much less than the channel length $L$, and, thus, the depletion charge enclosed by these sections are much smaller than the total depletion charge under the gate.
- However, for a short channel device, the widths of these depletion regions are a non-negligible fraction of the total depletion charge under the gate.
- Note: essentially, the depletion regions near the source and the drain are contributed by the source-substrate and the drain-substrate bias, and gate has no role to play.
• Under an applied drain-source bias, the depletion region thickness near the drain will obviously be larger than that at the source side.

• The net effect is that the gate now has to compensate for a lower depletion charge density than that for a long channel device, which qualitatively explains the reduction of the threshold voltage with a reduction in the channel length.

• The exact analysis of the charge sharing effects requires a two-dimensional analysis, however, to the first order, it is assumed that the effect of the depletion width \( d_{dd} \) at the drain side of the channel is to reduce the effective channel length in the saturation region from \( L \) to \( L_{eff} \), where

\[
L_{eff} = L - \Delta L
\]  
(5.46)

• Here, \( L_{eff} \) is the effective channel length, and the voltage dropped along this section is assumed to be equal to the drain saturation voltage \( V_{Dsat} \), and \( \Delta L \) is length of the pinched-off portion of the channel (related to the drain depletion width), where the excess drain voltage beyond \( V_{Dsat} \), i.e., \( V_D - V_{Dsat} \) is dropped, where \( V_D \) is the applied drain voltage.

• With an increase in \( V_{ds} \), the length of the pinch-off region \( \Delta L \) also increases, leading to a reduction in the effective channel length \( L_{eff} \).

• This effect is called the channel length modulation effect, and this effect leads to a higher drain saturation current, and finite output conductance \( (\partial I_{Dsat}/\partial V_{ds}) \) in the saturation region.

• A very crude estimate of the pinch-off length \( \Delta L \) (also referred to as the drain region length) can be obtained from the solution of the one-dimensional Poisson's equation:

\[
\frac{dF}{dx} = -\frac{qN_A}{\varepsilon_s} \quad (5.47)
\]

with the boundary condition \( F = -F_s \) at \( x = L_{eff} \), which leads to

\[
F(x) = -\frac{qN_A(x - L_{eff})}{\varepsilon_s} - F_s \quad (5.48)
\]

and from the condition

\[
V_D - V_{Dsat} = -\int F(x)dx \bigg|_{L_{eff}}^{L} \quad (5.49)
\]

the following quadratic expression is obtained for \( \Delta L \):

\[
\frac{qN_A}{2\varepsilon_s} (\Delta L)^2 + F_s \Delta L = V_D - V_{Dsat} \quad (5.50)
\]
A more accurate and realistic expression for $\Delta L$ may be obtained by assuming that the electrons are injected from the inversion layer into the drain depletion region, and they spread uniformly, leading to the current density

$$J = \frac{I_{ds}}{W \gamma Y}$$

(5.51)

where

$$\gamma = \frac{D_d - d_{inv} (x - L_{eff})}{\Delta L} + d_{inv}$$

(5.52)

Here, $D_d$ is the diffusion depth of the $n^+$ drain region, and $d_{inv}$ is the thickness of the inversion layer ($\sim 50-100$ Å). It is also assumed that the velocity of electrons in this region is saturated, thus their volume density can be given by $n = J/(q \phi_s)$.

Now, the one-dimensional Poisson's equation can be rewritten as:

$$\frac{dF}{dx} = -\frac{q \left[ N_A + \frac{J}{q \phi_s} \right]}{\varepsilon_s}$$

(5.53)

The solution of this equation leads to the following complicated expression for $\Delta L$:

$$\frac{q N_A}{2 \varepsilon_s} (\Delta L)^2 \left[ \frac{2 \xi_s \left( \ln \frac{D_d}{d_{inv}} - 1 \right)}{qN_A \gamma Y S_d} + F_s \Delta L - V_D - \sqrt{v_{sat}} \right]$$

(5.54)

For gate lengths larger than or about 1 μm, and drain-to-source voltages smaller than or about 10 V, this expression may be simplified to give
In short channel devices, the depletion charge under the channel [dependent on the channel potential and has been represented by the second term within the brackets in the right-hand side of Eq.(5.7)], which has been neglected in the charge control model [Eq.(5.19)], has to be accounted for.

This effect may be taken into account by introducing an additional parameter $a$ into the equations of the charge control model, with the resulting equations given by

**Linear Region** ($V_D < V_{Dsat}$)

$$I_D = k_N \left( V_g, V_D - \frac{aV_D^2}{2} \right)$$  (5.58)

**Saturation Region** ($V_D > V_{Dsat}$)

$$I_D = k_{NS} \left( V_g, V_{Dsat} - \frac{aV_D^2}{2} \right)$$  (5.59)

where $k_{NS} = \mu_n C_i (W/L_m)$ is the transconductance for the saturation region, and

$$V_{Dsat} = \frac{V_g}{a} + V_{SL} - \left( \frac{V_g}{a} \right)^2 + V_{SL}^{-1/2}$$  (5.60)

For Si, the (empirical and fitting) parameter $a$ describes the influence of the bulk substrate depletion layer on the device characteristics, and can be approximated by the following expression
The threshold voltage $V_T$ and the parameter $K$ can be determined from the experimentally measured data for a given device.

In addition, the dependence of electron mobility on the longitudinal and transverse electric field in the channel should be included for a more realistic device modeling, however, this simple empirical model gives adequately good fit with the measured data.

![Fig.5.18 The measured and calculated I-V characteristics for a Si n-channel MOSFET.](image)

Similar to the short channel device, the threshold voltage of a narrow channel (along the width) device increases with a reduction in the effective device width $W_{eff}$ due to the fringing fields outside the gate region, and the change in the threshold voltage as a function of $W_{eff}$ can be given by

$$
\Delta V_T = \frac{K_1 (2\Phi_b - V_{sub})}{W_{eff}}
$$

where $K_1$ is a constant.
Another non-ideal effect that may be especially important for short-channel devices is the injection of electrons from the channel directly to the gate dielectric, where these electrons get trapped => hot electron effect.

This phenomenon takes place because the carriers gain sufficient energy while traversing the drain depletion region, which contains a high electric field, and has been used to advantage in the FAMOS (Floating gate avalanche MOS) structures used in memories.

Avalanche breakdown of the drain-substrate junction can cause a sharp increase in the drain current, and can damage the device unless it is controlled by some external means.

Typically, avalanche breakdown for a heavily doped drain-moderately doped substrate junction takes place at approximately 8 to 10 V.

Another very important nonideal and potentially hazardous situation may arise due to punchthrough, where the drain and source depletion regions touch each other and cause abnormally large current to flow through the device: this effect is particularly severe for short channel devices.

Punchthrough effect creates a superlinear increase in the drain current with the drain voltage, even at gate voltages below the threshold voltage.

Subthreshold Conduction

So far, we have considered current flow in a MOSFET only when the gate voltage exceeds the threshold voltage.

However, in reality, a finite (nonzero) current does flow in a MOSFET even for gate voltages below the threshold voltage, and this effect is more marked for short channel length devices than their long channel counterparts.

This current is referred to as the subthreshold current, and it flows for $\phi_b < \phi_s < 2\phi_b$, i.e., when the surface potential lies between the ranges of the onset of weak inversion and the onset of strong inversion.

The mechanism responsible for subthreshold current is quite different for long-channel and short-channel devices. 5.6.1 Subthreshold Current in a Long Channel Device
- In a long channel device, the situation is similar to a BJT, where the source plays the role of the emitter, the drain is equivalent to the collector, and the substrate is the base.
- The drain voltage drops almost entirely across the drain-substrate depletion region.
- Thus, the component of the electric field parallel to the Si-SiO₂ interface is small, and the subthreshold current is contributed primarily by diffusion, just as the case for BJTs.

![Depletion regions](image.png)

**Fig. 5.20** The depletion regions associated with a (a) long channel and (b) short channel device.

- Thus, the subthreshold current can be evaluated as

\[
I_{\text{sub}} = -qA_{\text{eff}} \frac{dn}{dx}
\]  

(6.63)

where \( A_{\text{eff}} (= Wd_c) \) is the region where most electrons are located (the effective cross-sectional area).
The electron density $n$ at the surface is proportional to $e^{qV/kT}$, and it decreases with $y$ (perpendicular to the Si-SiO$_2$ interface) proportionally to $e^{-qF_y'y/kT}$, where $F_y$ is the vertical electric field, given by

$$F_y = \frac{Q_{dep}'}{\varepsilon_s} = \sqrt{\frac{2\varepsilon_s N_A}{\varepsilon_s}}$$  \hspace{1cm} (5.64)

Thus, the effective depth $d_e$, where most of the electrons are concentrated, can be estimated as $d_e \approx kT/qF_y(0)$, where $y = 0$ corresponds to the Si-SiO$_2$ interface.

If the diffusion length of electrons in the substrate $L_{nd}$ is much greater than the channel length $L$, then the electron density $n$ should be a linear function of $x$, decreasing from the source towards the drain (just like the linear distribution of minority carriers in the base of a BJT):

$$n(x) = n_{sd} - \frac{(n_{sd} - n_{dd})x}{L}$$  \hspace{1cm} (5.65)

where the volume concentrations for electrons $n_{sd}$ and $n_{dd}$ at the source and the drain sides of the channel are given by

$$n_{sd} = n_p 0 e^{qV(y)/kT} \quad \text{and} \quad n_{dd} = n_p 0 e^{q(V(y) - V_A)/kT}$$  \hspace{1cm} (5.66)

where $V(y)$ is the potential given by $V(y) \approx V_s - F_y y$, and $L_{1}$ is the length of the undepleted portion of the channel.

For long channel devices, it is assumed that the depletion widths at the source and the drain sides of the channel are small compared to the channel length $L$, and $L_1 \approx L$.

Also, note that since $n_{dd} \ll n_{sd}$, $n(x) \approx n_{sd}(1 - x/L)$.

Using all the relations given above, the subthreshold current for a long channel MOSFET can be given by

$$I_{sub} = \varepsilon_s h n \frac{W}{L} \sqrt{V_{th} \left( \frac{n_i}{N_A} \right)^2 \left( \frac{V_{th}}{V_s} \right)^2} \frac{e^{q(V_A)/kT}}{\varepsilon_s \sqrt{2L_{D_e}}} \left[ 1 - e^{-qV_A/kT} \right]$$  \hspace{1cm} (6.67)

The surface potential $V_s$ at the source can be expressed as a function of the gate voltage by noting that $V_g = V_{FB} + V_t + V_s$, where $V_t = \varepsilon_s F_y D_0/C_f$, thus,

$$V_s = V_g - V_{FB} + A_s^2 - A_s \left[ A_s^2 + 2(V_g - V_{FB}) \right]^{1/2}$$  \hspace{1cm} (6.68)
where \( a_s = \frac{(qN_A)^{1/2}}{C_I} \).

- Note: For \( V_D > 3V_{th} \), the subthreshold current becomes independent of the drain voltage.
- This is expected since in a long channel device, most of the applied drain voltage drops at the drain-substrate depletion region, and since the current is diffusive in nature, there is no change in the current with the drain voltage.
- Also, for large \( V_D \), since \( n_{dd} << n_{sd} \), the gradient of \( n \) is not affected by the drain voltage: a situation similar to BJTs, where the collector current in the forward active mode is independent of the collector-to-emitter voltage.
- Note: the subthreshold current is almost independent of the drain voltage \( V_D \).
- The substrate bias shifts the threshold voltage to a more positive value, affects the surface potential, and thus the subthreshold current changes.

![Fig.5.21](image)

**Fig.5.21** The subthreshold characteristics for a long channel device as a function of the gate voltage for different values of drain and substrate voltages.

**Subthreshold Current in a Short Channel Device**

- In a short channel device, the source and drain depletion widths \( d_{sd} \) and \( d_{dd} \) may be a significant portion of the channel length \( L \), and, hence, can not be neglected.
- To account for this effect, the term \( L \) in Eq.(5.67) is replaced by another term \( L_{eff} \), where \( L_{eff} = L - d_{sd} - d_{dd} \), where

\[
\begin{align*}
    d_{sd} &= \sqrt{\frac{2\varepsilon_s (V_{bi} - V_s)}{qN_A}} \\
    d_{dd} &= \sqrt{\frac{2\varepsilon_s (V_{bi} - V_s + V_D)}{qN_A}}
\end{align*}
\]  

\((5.69)\)
where $V_b$ is the built-in voltage of the n$^+$-source/drain-substrate junction, and the surface potential $V_s$ is now found from the solution of the following equation:

$$V_s = V_g - V_{FB} - \frac{\sqrt{4\varepsilon_s N_A (V_g - V_{sub})}}{C_i} \left[ 1 + \frac{L - W_{ds} - W_{dd}}{L - d_{sd} - d_{dd}} \right]$$  \hspace{1cm} (5.70)

where

$$W_{ds} = \sqrt{\frac{2\varepsilon_s (V_{bi} - V_{sub})}{qN_A}} \quad \text{and} \quad W_{dd} = \sqrt{\frac{2\varepsilon_s (V_{bi} - V_{sub} + V_D)}{qN_A}}$$  \hspace{1cm} (5.71)

- The curves clearly show shifts in the subthreshold current for different values of drain voltages, a characteristic typical of short channel devices.
- The subthreshold current is a strong function of temperature as well ($e^{1/T}$ dependence).

Fig.5.22 The subthreshold characteristics for a short channel device as a function of gate voltage for different values of drain and substrate voltages.
Fig. 5.23 The subthreshold characteristics as a function of gate voltage for two different temperatures (77 K and 300 K).

**MOSFET Capacitances and Equivalent Circuit**

- Note: in a MOSFET, the charges in the depletion region and the inversion layer depend on the gate, source, drain, and substrate potentials; and the derivatives of these charges with respect to the terminal voltages give rise to MOSFET capacitances.
- The small signal equivalent circuit shown in Fig. 5.24 is the one used by the popular circuit simulation package called SPICE, and it contains:
  - the drain-to-source current source $I_{DS}$,
  - two resistances $R_S$ and $R_D$ (due to the quasi-neutral region resistances of the source and drain respectively)

The gate-to-drain capacitance $C_{gd} = C_{gd(overlap)} = 1 \text{ fF}$.

The gate-to-body capacitance $C_{gb} = 0$ (in saturation).

The source-to-substrate capacitance

$$C_{sb} = \frac{C_{sb0}}{1 - \left(\frac{V_{sb} - S}{V_{bi}}\right)^m} = 12.25 \text{ fF}.$$  

The drain-to-substrate capacitance
Note: in the presence of series source/drain resistances \( R_s \) and \( R_d \), the intrinsic (internal to the device) conductance \( g_{d0} \) and transconductances \( (g_{m0} \text{ and } g_{mb0}) \) are related to the extrinsic (measured) transconductances \( (g_m \text{ and } g_{mb}) \) and conductance \( (g_d) \) by the following equation:

\[
\frac{g_m}{g_{m0}} = \frac{g_d}{g_{d0}} = \frac{g_{mb}}{g_{mb0}} = \frac{1}{1 + R_s (g_{m0} + g_{mb0}) + g_{d0} (R_s + R_d)}
\]

\((5.83)\)

**EXAMPLE 5.3:** An n-channel MOSFET has \( g_{m0} = 0.1 \text{ mA/V} \), \( g_{d0} = 20 \mu\text{A/V} \), and \( \chi = 0.3 \). Determine \( g_m \), \( g_{mb} \), and \( g_d \) for \( R_s = R_d = 50 \Omega \) and 500 \( \Omega \).

**SOLUTION:** The intrinsic body transconductance \( g_{mb0} = \chi g_{m0} = 30 \mu\text{A/V} \).

The coefficient

\[
\frac{1}{1 + R_s (g_{m0} + g_{mb0}) + g_{d0} (R_s + R_d)} = 0.99 \text{ for } R_s = R_d = 50 \Omega, \text{ and } \\
= 0.92 \text{ for } R_s = R_d = 500 \Omega.
\]
Therefore, \( g_m = 99 \text{ } \mu\text{A/\text{V}} \) and \( 92 \text{ } \mu\text{A/\text{V}} \), \( g_{mb} = 29.7 \text{ } \mu\text{A/\text{V}} \) and \( 27.6 \text{ } \mu\text{A/\text{V}} \), and \( g_d = 19.8 \text{ } \mu\text{A/\text{V}} \) and \( 18.4 \text{ } \mu\text{A/\text{V}} \) for \( R_s = R_d = 50 \text{ } \Omega \) and \( 100 \text{ } \Omega \), respectively. Thus, significant degradation in the transconductances and drain conductance may take place for large values of source/drain series resistances.

- The two conductance terms \( g_{bd} \) and \( g_{bs} \) appearing in the equivalent circuit shown in Fig.5.26(a) are the reverse-bias conductances of the source-substrate and drain-substrate diodes, and their values are very small (tending to zero).

![Simplified equivalent circuit of a MOSFET](image)

Fig.5.26(b) The simplified equivalent circuit of a MOSFET.

- A simplified equivalent circuit is shown in Fig.5.26(b).
- For the circuit shown in Fig.5.26(b), the small signal voltage gain expression can be given by:

\[
A_v = \frac{V_o}{V_i} = \frac{-g_m + j\omega C_{gd}}{g_d + j\omega C_{gd}}
\]

(5.84)

- Note: at low frequencies, when the effects of the capacitances can be neglected, the voltage gain can be given by \( A_v \approx -g_m/g_d \) as expected.
- Another simplified equivalent circuit, suitable for the calculation of the current gain, is shown in Fig.5.26(c).
Fig. 5.26(c) The alternate simplified equivalent circuit for a MOSFET suitable for the calculation of the short circuit current gain.

- From Fig. 5.26(c), the short circuit current gain can be easily found to be:

\[ A_I = \frac{i_L}{i} = \frac{-g_m}{j\omega(C_{gs} + C_{gd})} \]  \hspace{1cm} (6.85)

- Thus, the unity gain cutoff frequency (i.e., the frequency at which the absolute value of the short circuit current gain is equal to unity) \( f_T \) can be given by

\[ f_T = \frac{g_m}{2\pi C_g} \]  \hspace{1cm} (6.86)

where \( C_g = C_{gs} + C_{gd} \).

- Now, note that \( C_{gs} \gg C_{gd} \), and \( C_{gs} \simeq C_i \) in the strong inversion region.
- Also, the drain current \( I_d = qn_s \nu_{eff} W \) (electrons in transit model), with \( n_s = Q_0/(WL) \).
- Thus, \( g_m = (\partial P/\partial V_d) = (\partial Q_0/\partial V_d) \nu_{eff} L \approx C_i \nu_{eff} L \).
- Hence,

\[ f_T = \nu_{eff} \frac{L}{2\pi} = \frac{1}{2\pi \tau_f} \]  \hspace{1cm} (5.87)

where \( \tau_f = \frac{L}{V_{eff}} \) is the transit time of electrons in the channel.

- This equation gives the theoretical maximum value for \( f_T \).
- Assuming \( \nu_{eff} \approx 5 \times 10^4 \text{ m/sec} \), the characteristic switching time for a MOSFET is obtained as \( t_s \approx \tau_f \text{ (psec)} \approx 20/L \text{ (\mu m)} \) and \( f_T \text{ (GHz)} \approx 8/L \text{ (\mu m)} \).
In reality, the measured switching times for MOSFETs are at least several times larger than that predicted above due to the parasitic and fringing capacitances that has to be added to the gate capacitance \( C_G \), leading to the following modified expression for \( f_T \):

\[
\frac{g_m}{2\pi(C_g + C_p)} = \frac{1}{2\pi f_T |1 + C_p / C_g|}
\]

EXAMPLE 5.4: Calculate the unity-gain cutoff frequency \( f_T \) for the MOSFET considered in Example 5.2. Compare this value with theoretical maximum value for \( f_T \), assuming \( v_{\text{eff}} = 5 \times 10^4 \text{ m/sec} \).

**SOLUTION:** The unity-gain cutoff frequency

\[
f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} = 2.82 \text{ GHz}.
\]

The theoretical maximum value for \( f_T = \frac{v_{\text{eff}}}{2\pi L} = 7.96 \text{ GHz} \).

An actual device would show a cutoff frequency, which is smaller of the two, thus, the actual unity-gain cutoff for the device considered in Example 5.2 would be 2.82 GHz.

**Types of MOSFETs**

- Broadly, MOSFETs can be categorized into two types: enhancement and depletion.
- Enhancement type devices are normally off, i.e., channel does not exist for \( V_{gs} = 0 \), and the applied \( |V_{gs}| \) must be greater than \( V_T \) for the device to turn on.
- On the other hand, depletion type devices are normally on, i.e., channel does exist even for \( V_{gs} = 0 \) and the applied \( |V_{gs}| \) must be reduced below \( V_T \) for the device to turn off.
- To put it simply, an n-channel enhancement type device has a positive \( V_T \), whereas an n-channel depletion type device has a negative \( V_T \).
- Similarly, a p-channel enhancement type device has a negative \( V_T \), whereas a p-channel depletion type device has a positive \( V_T \).
- The threshold voltage can be changed either by doping or by ion implantation, where high energy ions are made to bombard the surface and get embedded into it: since these are charged, they can change the charge state of the surface, and, hence, the threshold voltage.
The shift in the threshold voltage $\Delta V_T$ is related to the ion density $\Delta Q_i^f$ by the relation: $\Delta V_T = \Delta Q_i^f / C_i^f$. For example, negative ions (like Boron) implanted in a p-channel (n-substrate) device will compensate some of the positive depletion charges and make the threshold voltage less negative, however, note the same ions would shift the threshold voltage to more positive for n-channel (p-substrate) device.

**EXAMPLE 5.5:** An n-channel MOSFET with $t_{ox} = 30$ nm has a threshold voltage $V_T = 1$ V. Determine the type and dose (in numbers/cm$^2$) of ion implantation required to make it a depletion mode device with $V_T = -0.5$ V.

**SOLUTION:** The oxide capacitance per unit area $C_i^f = \varepsilon_{ox} A_{ox} = 1.15 \times 10^{-7}$ F/cm$^2$.

The dose of ion implantation required $N_i^f = |\Delta Q_i^f| / q = |\Delta V_T| C_i^f / q$

$= 1.08 \times 10^{12}$ cm$^{-2}$.

Since the threshold voltage is shifting towards negative value, hence, obviously, the type of implant required is positive ions (e.g., P, As, Sb, etc.), which would compensate the negative depletion charge of the substrate and push the threshold voltage towards negative direction.