Computer Architecture
Code: IT502
Contact: 3L + 1T
Credits: 4

Pre-requisite: Basic Electronics in First year, Introduction to Computing in second semester, Analog & Digital Electronics and Computer Organisation in Third semester.

Module – 1: [12 L]
Introduction: Review of basic computer architecture (Revisited), Quantitative techniques in computer design, measuring and reporting performance. (3L)

Pipelining: Basic concepts, instruction and arithmetic pipeline, data hazards, control hazards and structural hazards, techniques for handling hazards. Exception handling. Pipeline optimization techniques; Compiler techniques for improving performance. (9L)

Module – 2: [8L]
Hierarchical memory technology: Inclusion, Coherence and locality properties; Cache memory organizations, Techniques for reducing cache misses; Virtual memory organization, mapping and management techniques, memory replacement policies. (8L)

Module – 3: [6L]
Instruction-level parallelism: basic concepts, techniques for increasing ILP, superscalar, superpipelined and VLIW processor architectures. Array and vector processors. (6L)

Module – 4: [12 L]
Multiprocessor architecture: taxonomy of parallel architectures; Centralized shared- memory architecture: synchronization, memory consistency, interconnection networks. Distributed shared-memory architecture. Cluster computers. (8L)

Non von Neumann architectures: data flow computers, reduction computer architectures, systolic architectures. (4L)